CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH	A. toggle B. set C. reset D. not change
2	What is the difference between a D latch and a D flip-flop?	A. The D latch has a clock input B. The D flip-flop has an enable input C. The D latch is used for faster operation D. The D flip-flop has a clock input
3	The storage cell in SRAM is	A. a flip –flop B. a capacitor C. a fuse D. a magnetic domain
4	The 4-bit 2"s complement representation of "+5" is _____	A. 1010 B. 1110 C. 1011 D. 0101
5	FIFO is an acronym for _____	A. First In, First Out B. Fly in, Fly Out C. Fast in, Fast Out D. None of given options
6	The alternate solution for a demultiplexer-register combination circuit is _____	A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
7	_____ is used to minimize the possible no. of states of a circuit.	A. State assignment B. State reduction C. Next state table D. State diagram
8	A synchronous decade counter will have _____ flip-flops.	A. 3 B. 4 C. 7 D. 10
9	74HC163 has two enable input pins which are _____ and _____	A. ENP, ENT B. ENl, ENC C. ENP, ENC D. ENT, ENl
10	_____ counters as the name indicates are not triggered simultaneously.	A. Asynchronous B. Synchronous C. Positive-Edge triggered D. Negative-Edge triggered