CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid
2	WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO.	A. THE FLOP-FLOP IS TRIGGERED B. Q=0 AND Q"=1 C. Q=1 AND Q'=0 D. THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED
3	Sum term (Max term) is implemented using _____ gates	A. OR B. AND C. NOT D. OR-AND
4	In designing any counter the transition from a current state to the next sate is determined by	A. Current state and inputs B. Only inputs C. Only current state D. current state and outputs
5	The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms	A. 4 B. 8 C. 12 D. 16
6	Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer	A. A parallel to serial converter circuit B. A counter circuit C. A BCD to Decimal decoder D. A 2-to-8 bit decoder
7	The power dissipation, PD, of a logic gate is the product of the	A. dc supply voltage and the peak current B. dc supply voltage and the average supply current C. ac supply voltage and the peak current D. ac supply voltage and the average supply current
8	Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.	A. A = 1, B = 0, C = 0, D = 0 B. A = 1, B = 0, C = 1, D = 0 C. A = 0, B = 1, C = 0, D = 0 D. A = 1, B = 0, C = 1, D = 1
9	If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be	A. set B. reset C. invalid D. clear
10	The OR gate performs Boolean _____.	A. multiplication B. subtraction C. division D. addition