CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	The design and implementation of synchronous counters start from _____	A. Truth table B. state diagram C. k-map D. state table
2	THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____	A. GATED FLIP-FLOPS B. PULSE TRIGGERED FLIP-FLOPS C. POSITIVE-EDGE TRIGGERED FLIP-FLOPS D. NEGATIVE-EDGE TRIGGERED FLIP-FLOPS
3	A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?	A. = 0, Cout = 0 B. = 0, Cout = 1 C. = 1, Cout = 0 D. = 1, Cout = 1
4	The alternate solution for a multiplexer and a register circuit is _____	A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
5	Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state	A. Ten B. Eight C. Three D. Two
6	The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines	A. Write Time B. Recycle Time C. Refresh Time D. Access Time
7	In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.	A. Moore machine B. Mealy machine C. Johnson counter D. Ring counter
8	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status	A. 3 B. 7 C. 8 D. 15
9	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____	A. Using S-R Flop-Flop B. D-flipflop C. J-K flip-flop D. T-Flip-Flop
10	If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid