CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	In _____ the Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop.	A. Moore machine B. Mealy machine C. Johnson counter D. Ring counter
2	At T0 the value stored in a 4-bit left shift was “1”. What will be the value of register after three clock pulses?	A. 2 B. 4 C. 6 D. 8
3	A synchronous decade counter will have _____ flip-flops	A. 3 B. 4 C. 7 D. 10
4	A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.	A. 10 Hz B. 50 Hz C. 100 Hz D. 500 Hz
5	A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.	A. 3 B. 7 C. 8 D. 15
6	A negative edge-triggered flip-flop changes its state when _____	A. Enable input (EN) is set B. Preset input (PRE) is set C. Low-to-high transition of clock D. High-to-low transition of clock
7	A positive edge-triggered flip-flop changes its state when _____	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
8	Demultiplexer converts _____ data to _____ data.	A. Parallel data, serial data B. Serial data, parallel data C. Encoded data, decoded data D. All of the given options
9	The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?	A. A > B = 1, A < B = 0, A < B = 1 B. A > B = 0, A < B = 1, A = B = 0 C. A > B = 1, A < B = 0, A = B = 0 D. A > B = 0, A < B = 1, A = B = 1
10	The OR Gate performs a Boolean _____ function	A. Addition B. Subtraction C. Multiplication D. Division