

CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	A GAL is essentially a _____.	A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL
2	A multiplexer with a register circuit converts _____	A. Serial data to parallel B. Parallel data to serial C. Serial data to serial D. Parallel data to parallel
3	The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____	A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs
4	LUT is acronym for _____.	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
5	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)	A. 1100 B. 0011 C. 0000 D. 1111
6	_____ is used to simplify the circuit that determines the next state.	A. State diagram B. Next state table C. State reduction D. State assignment
7	In a state diagram, the transition from a current state to the next state is determined by	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
8	Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____	A. 0000 B. 1101 C. 1011 D. 1111
9	_____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	A. Race condition B. Clock Skew C. Ripple Effect D. None of given options
10	_____ is one of the examples of synchronous inputs.	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)