

CS-302 Quiz Preparation Virtual University

Sr	Questions	Answers Choice
1	A 8-bit serial in / parallel out shift register contains the value "8", clock signal(s) will be required to shift the value completely out of the register.	A. 1 B. 2 C. 4 D. 8
2	In a sequential circuit the next state is determined by and	A. State variable, current state B. Current state, flip-flop output C. Current state and external input D. Input and clock signal applied
3	The divide-by-60 counter in digital clock is implemented by using two cascading counters:	A. Mod-6, Mod-10 B. Mod-50, Mod-10 C. Mod-10, Mod-50 D. Mod-50, Mod-6
4	The minimum time for which the input signal has to be maintained at the input of flip-flop is called of the flip-flop.	A. Set-up time B. Hold time C. Pulse Interval time D. Pulse Stability time
5	74HC163 has two enable input pins which are and	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
6	is said to occur when multiple internal variables change due to change in one input variable.	A. Clock Skew B. Race condition C. Hold delay D. Hold and Wait
7	The input overrides the input.	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
8	A decade counter is	A. Mod-3 counter B. Mod-5 counter C. Mod-8 counter D. Mod-10 counter
9	In asynchronous transmission when the transmission line is idle,	 A. It is set to logic low B. It is set to logic high C. Remains in previous state D. State of transmission line is not used to start transmission
10	A Nibble consists of bits	A. 2 B. 8 C. 4 D. 16
11	Excess-8 code assigns to "-8"	A. 1110 B. 1100 C. 1000 D. 0000
12	The voltage gain of the Inverting Amplifier is given by the relation	A. Vout / Vin = - Rf / Ri B. Vout / Rf = - Vin / Ri C. Rf / Vin = - Ri / Vout D. Rf / Vin = Ri / Vout
13	LUT is acronym for	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
14	The three fundamental gates are	A. AND, NAND, XOR B. OR, AND, NAND C. NOT, NOR, XOR D. NOT, OR, AND
		A. The organization of memory

15	The total amount of memory that is supported by any digital system depends upon	B. The structure of memoryC. The size of decoding unitD. The size of the address bus of the microprocessor
16	Stack is an acronym for	A. FIFO memory B. LIFO memory C. Flash Memory D. Bust Flash Memory
17	Addition of two octal numbers "36" and "71" results in	A. 213 B. 123 C. 127 D. 345
18	is one of the examples of synchronous inputs.	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)
19	occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	A. Race condition B. Clock Skew C. Ripple Effect D. None of given options
20	Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be	A. 0000 B. 1101 C. 1011 D. 1111
21	In a state diagram, the transition from a current state to the next state is determined by	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
22	is used to simplify the circuit that determines the next state.	A. State diagram B. Next state table C. State reduction D. State assignment
23	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)	A. 1100 B. 0011 C. 0000 D. 1111
24	LUT is acronym for	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
24 25	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs
24 25 26	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop A multiplexer with a register circuit converts	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs A. Serial data to parallel B. Parallel data to serial C. Serial data to parallel D. Parallel data to parallel
24 25 26 27	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop A multiplexer with a register circuit converts A GAL is essentially a	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs A. Serial data to parallel B. Parallel data to serial C. Serial data to serial D. Parallel data to parallel A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL
24 25 26 27 28	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop A multiplexer with a register circuit converts A GAL is essentially a in, all the columns in the same row are either read or written.	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs A. Serial data to parallel B. Parallel data to serial C. Serial data to parallel D. Parallel data to parallel A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL A. Sequential Access B. MOS Access C. FAST Mode Page Access D. None of given options
24 25 26 27 28 29	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop A multiplexer with a register circuit converts A GAL is essentially a in, all the columns in the same row are either read or written. In order to synchronize two devices that consume and produce data at different rates, we can use	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs A. Serial data to parallel B. Parallel data to serial C. Serial data to serial D. Parallel data to parallel A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL B. MOS Access C. FAST Mode Page Access D. None of given options A. Read Only Memory B. Fist In First Out Memory C. Flash Memory D. Fast Page Access Mode Memory
24 25 26 27 28 29 30	LUT is acronym for The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop A multiplexer with a register circuit converts A GAL is essentially a in, all the columns in the same row are either read or written. In order to synchronize two devices that consume and produce data at different rates, we can use A positive edge-triggered flip-flop changes its state when	 A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options A. Doesn't have an invalid state B. Sets to clear when both J = 0 and K = 0 C. It does not show transition on change in pulse D. It does not accept asynchronous inputs A. Serial data to parallel B. Parallel data to serial C. Serial data to serial D. Parallel data to serial D. Parallel data to parallel A. Non-reprogrammable PAL B. PAL that is programmed only by the manufacturer C. Very large PAL D. Reprogrammable PAL A. Sequential Access B. MOS Access C. FAST Mode Page Access D. None of given options A. Read Only Memory B. Fist In First Out Memory C. Flash Memory D. Fast Page Access Mode Memory A. Low-to-high transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set

32	In a sequential circuit the next state is determined by and	A. State variable, current state B. Current state, flip-flop output C. Current state and external input D. Input and clock signal applied
33	The divide-by-60 counter in digital clock is implemented by using two cascading counters	A. Mod-6, Mod-10 B. Mod-50, Mod-10 C. Mod-10, Mod-50 D. Mod-50, Mod-6
34	Flip flops are also called	 A. Bi-stable dualvibrators B. Bi-stable transformer C. Bi-stable multivibrators D. Bi-stable singlevibrators
35	74HC163 has two enable input pins which are and	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
36	is said to occur when multiple internal variables change due to change in one input variable	A. Clock Skew B. Race condition C. Hold delay D. Hold and Wait
37	Given the state diagram of an up/down counter, we can find	 A. The next state of a given present state B. The previous state of a given present state C. Both the next and previous states of a given state D. The state diagram shows only the inputs/outputs of a given states
38	The input overrides the input	A. Asynchronous, synchronous B. Synchronous, asynchronous C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)
39	A logic circuit with an output consists of	 A. two AND gates, two OR gates, two inverters B. three AND gates, two OR gates, one inverter C. two AND gates, one OR gate, two inverters D. two AND gates, one OR gate
40	In asynchronous transmission when the transmission line is idle,	 A. It is set to logic low B. It is set to logic high C. Remains in previous state D. State of transmission line is not used to start transmission
41	LUT is acronym for	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
42	DRAM stands for	A. Dynamic RAMB. Data RAMC. Demoduler RAMD. None of given options
43	The expression F=A+B+C describes the operation of three bits Gate	A. OR B. AND C. NOT D. NAND
44	Stack is an acronym for	A. FIFO memory B. LIFO memory C. Flash Memory D. Bust Flash Memory
45	The ANSI/IEEE Standard 754 defines aSingle-Precision Floating Point format for binary numbers.	A. 8-bit B. 16-bit C. 32-bit D. 64-bit
46	The decimal "17" in BCD will be represented as	A. ₁₁₁₀₁ B. 11011 C. 10111 D. 11110
A7	The basis basisted black for a factor factor f	A. A Flip-Flop B. A Logical Gate

D. None of given options

41	I ne basic building block for a logical circuit is	C. An Adder D. None of given options
48	The output of the expression F=A.B.C will be Logic when A=1, B=0, C=1	A. Undefined B. One C. Zero D. No Output as input is invalid
49	is invalid number of cells in a single group formed by the adjacent cells in K-map	A. 2 B. 8 C. 12 D. 16
50	The PROM consists of a fixed non-programmable Gate array configured as a decoder	A. AND B. OR C. NOT D. XOR
51	is one of the examples of synchronous inputs	A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)
52	is one of the examples of asynchronous inputs.	A. J-K input B. S-R input C. D input D. Clear Input (CLR)
53	In a state diagram, the transition from a current state to the next state is determined by.	A. Current state and the inputs B. Current state and outputs C. Previous state and inputs D. Previous state and outputs
54	is used to minimize the possible no. of states of a circuit.	A. State assignment B. State reduction C. Next state table D. State diagram
55	The best state assignment tends to	 A. Maximizes the number of state variables that don't change in a group of related states B. Minimizes the number of state variables that don"t change in a group of related states C. Minimize the equivalent states D. None of given options
56	5-bit Johnson counter sequences through states	A. 7 B. 10 C. 32 D. 25
57	Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse?	A. 1100 B. 0011 C. 0000
58	The address from which the data is read, is provided by	A. Depends on circuitry B. None of given options C. RAM D. Microprocessor
59	FIFO is an acronym for	A. First In, First Out B. Fly in, Fly Out C. Fast in, Fast Out D. None of given options
60	of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.	A. Resolution B. Missing Code C. Accuracy D. Quantization
61	Above is the circuit diagram of	A. Asynchronous up-counter B. Asynchronous down-counter C. Synchronous up-counter D. Synchronous down-counter
62	The sequence of states that are implemented by a n-bit Johnson counter is	A. n+2 (n plus 2) B. 2n (n multiplied by 2) C. 2n (2 raise to power n) D. n2 (n raise to power 2)
63	"A + B = B + A" is	A. Demorgan"s Law B. Distributive Law C. Commutative Law D. Associative Law
		A. Using a single comparator

64	An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is	Comparators C. Connecting comparators in vertical hierarchy D. Extra logic gates are always required
65	Demultiplexer is also called.	A. Data selector B. Data router C. Data distributor D. Data encoder
66	A positive edge-triggered flip-flop changes its state when	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
67	A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is	A. 10 mW B. 25 mW C. 64 mW D. 1024
68	counters as the name indicates are not triggered simultaneously.	A. Asynchronous B. Synchronous C. Positive-Edge triggered D. Negative-Edge triggered
69	74HC163 has two enable input pins which are and	A. ENP, ENT B. ENI, ENC C. ENP, ENC D. ENT, ENI
70	A synchronous decade counter will have flip-flops.	A. 3 B. 4 C. 7 D. 10
71	is used to minimize the possible no. of states of a circuit.	A. State assignment B. State reduction C. Next state table D. State diagram
72	The alternate solution for a demultiplexer-register combination circuit is	 A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
73	FIFO is an acronym for	A. First In, First Out B. Fly in, Fly Out C. Fast in, Fast Out D. None of given options
74	The 4-bit 2"s complement representation of "+5" is	A. 1010 B. 1110 C. 1011 D. 0101
75	The storage cell in SRAM is	A. a flip –flop B. a capacitor C. a fuse D. a magnetic domain
76	What is the difference between a D latch and a D flip-flop?	A. The D latch has a clock input B. The D flip-flop has an enable input C. The D latch is used for faster operation D. The D flip-flop has a clock input
77	For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will if the clock goes HIGH	A. toggle B. set C. reset D. not change
78	The OR gate performs Boolean	A. multiplication B. subtraction C. division D. addition
79	If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be	A. set B. reset C. invalid D. clear
80	Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.	A. $A = 1$, $B = 0$, $C = 0$, $D = 0$ B. $A = 1$, $B = 0$, $C = 1$, $D = 0$ C. $A = 0$, $B = 1$, $C = 0$, $D = 0$ D. $A = 1$, $B = 0$, $C = 1$, $D = 1$

81	The power dissipation, PD, of a logic gate is the product of the	A. dc supply voltage and the peak current B. dc supply voltage and the average supply current C. ac supply voltage and the peak current D. ac supply voltage and the average supply current
82	Using multiplexer as parallel to serial converter requires connected to the multiplexer	 A. A parallel to serial converter circuit B. A counter circuit C. A BCD to Decimal decoder D. A 2-to-8 bit decoder
83	The 3-variable Karnaugh Map (K-Map) has cells for min or max terms	A. 4 B. 8 C. 12 D. 16
84	In designing any counter the transition from a current state to the next sate is determined by	A. Current state and inputsB. Only inputsC. Only current stateD. current state and outputs
85	Sum term (Max term) is implemented using gates	A. OR B. AND C. NOT D. OR-AND
86	WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO.	A. THE FLOP-FLOP IS TRIGGERED B. Q=0 AND Q"=1 C. Q=1 AND Q'=0 D. THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED
87	If S=1 and R=0, then Q(t+1) = for positive edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid
88	If S=1 and R=1, then Q(t+1) = for negative edge triggered flip-flop	A. 0 B. 1 C. Invalid D. Input is invalid
89	We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by	A. Using S-R Flop-Flop B. D-flipflop C. J-K flip-flop D. T-Flip-Flop
90	A counter is implemented using three (3) flip-flops, possibly it will have maximum output status	A. 3 B. 7 C. 8 D. 15
91	In Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.	A. Moore machine B. Meally machine C. Johnson counter D. Ring counter
92	The of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines	A. Write Time B. Recycle Time C. Refresh Time D. Access Time
93	Bi-stable devices remain in either of their states unless the inputs force the device to switch its state	A. Ten B. Eight C. Three D. Two
94	The alternate solution for a multiplexer and a register circuit is	 A. Parallel in / Serial out shift register B. Serial in / Parallel out shift register C. Parallel in / Parallel out shift register D. Serial in / Serial Out shift register
95	A full-adder has a Cin = 0. What are the sum (<private "type='PICT;ALT=sigma"'>) and the carry (Cout) when A = 1 and B = 1?</private>	A. = 0, Cout = 0 B. = 0, Cout = 1 C. = 1, Cout = 0 D. = 1, Cout = 1
96	THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A	A. GATED FLIP-FLOPS B. PULSE TRIGGERED FLIP-FLOPS C. POSITIVE-EDGE TRIGGERED FLIP-FLOPS D. NEGATIVE-EDGE TRIGGERED FLIP-FLOPS
		A. Truth table

97	The design and implementation of synchronous counters start from	C. k-map D. state table
98	The design and implementation of synchronous counters start from	A. state table B. k-map C. state diagram D. Truth table
99	THE HOURS COUNTER IS IMPLEMENTED USING	A. ONLY A SINGLE MOD-12 COUNTER IS REQUIRED B. MOD-10 AND MOD-6 COUNTERS C. MOD-10 AND MOD-2 COUNTERS D. A SINGLE DECADE COUNTER AND A FLIP-FLOP
100	LUT is acronym for	A. Look Up Table B. Local User Terminal C. Least Upper Time Period D. None of given options
101	of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output	A. Resolution B. Accuracy C. Quantization D. Missing Code
102	The high density FLASH memory cell is implemented using	A. 1 floating-gate MOS transistor B. 2 floating-gate MOS transistors C. 4 floating-gate MOS transistors D. 6 floating-gate MOS transistors
103	Q2 :=Q1 OR X OR Q3	A. Q2:= Q1 \$ X \$ Q3 B. Q2:= Q1 # X# Q3 C. Q2:= Q1 & & amp; X & amp; Q3 D. Q2:= Q1 ! X ! Q3
104	Generally, the Power dissipation of devices remains constant throughout their operation.	A. TTL B. CMOS 3.5 series C. CMOS 5 Series D. Power dissipation of all circuits increases with time
105	When the control line in tri-state buffer is high the buffer operates like agate	A. AND B. OR C. NOT D. XOR
106	3.3 v CMOS series is characterized by andas compared to the 5 v CMOS series	 A. Low switching speeds, high power dissipation B. Fast switching speeds, high power dissipation C. Fast switching speeds, very low power dissipation D. Low switching speeds, very low power dissipation
107	The output of an AND gate is one when	A. All of the inputs are one B. Any of the input is one C. Any of the input is zero D. All the inputs are zero
108	The OR Gate performs a Boolean function	A. Addition B. Subtraction C. Multiplication D. Division
109	The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?	A. A > B = 1, A < B = 0, A < B = 1 B. A > B = 0, A < B = 1, A = B = 0 C. A > B = 1, A < B = 0, A = B = 0 D. A > B = 0, A < B = 1, A = B = 1
110	Demultiplexer converts data to data.	 A. Parallel data, serial data B. Serial data, parallel data C. Encoded data, decoded data D. All of the given options
111	A positive edge-triggered flip-flop changes its state when	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
112	A negative edge-triggered flip-flop changes its state when	 A. Enable input (EN) is set B. Preset input (PRE) is set C. Low-to-high transition of clock D. High-to-low transition of clock

113	A counter is implemented using three (3) flip-flops, possibly it will have maximum output status.	A. 3 B. 7 C. 8 D. 15
114	A divide-by-50 counter divides the input signal to a 1 Hz signal.	A. 10 Hz B. 50 Hz C. 100 Hz D. 500 Hz
115	A synchronous decade counter will have flip-flops	A. 3 B. 4 C. 7 D. 10
116	At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?	A. 2 B. 4 C. 6 D. 8
117	In the Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop.	A. Moore machine B. Meally machine C. Johnson counter D. Ring counter
118	Which is not characteristic of a shift register?	A. Serial in/parallel in B. Serial in/parallel out C. Parallel in/serial out D. Parallel in/parallel out
119	The of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines.	A. Write Time B. Recycle Time C. Refresh Time D. Access Time
120	The output of an XNOR gate is 1 when I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one.	A. I Only B. IV Only C. I and IV only D. II and III only
121	NAND gate is formed by connecting	A. AND Gate and then NOT Gate B. NOT Gate and then AND Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate
122	Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be	A. Zero B. One C. Undefined D. No output as input is invalid
123	The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called	A. Radiation-Erase programming method (REPM) B. In-System Programming (ISP) C. In-chip Programming (ICP) D. Electronically-Erase programming method (EEPM)
124	The ABEL symbol for "OR" operation is	A. ! B. & C. # D. \$
125	For a gated D-Latch if EN=1 and D=1 then Q(t+1) =	A. 0 B. 1 C. Q(t) D. Invalid
126	A positive edge-triggered flip-flop changes its state when	A. Low-to-high transition of clock B. High-to-low transition of clock C. Enable input (EN) is set D. Preset input (PRE) is set
127	In outputs depend only on the combination of current state and inputs.	A. Mealy machine B. Moore Machine C. State Reduction table D. State Assignment table
128	In the following statement Z PIN 20 ISTYPE "reg.invert"; The keyword "reg.invert" indicates	A. An inverted register input B. An inverted register input at pin 20 C. Active-high Registered Mode output D. Active-low Registered Mode output
		A. It is locked: no data is allowed to

		memory and new data enters D. None of given options
130	The process of converting the analogue signal into a digital representation (code) is known as	A. Strobing B. Amplification C. Quantization D. Digitization
131	(A + B)(A + B + C)(A + C) is an example of	A. Product of sum form B. Sum of product form C. Demorgans law D. Associative law
132	Q2 :=Q1 OR X OR Q3 The above ABEL expression will be	A. Q2:= Q1 \$ X\$ Q3 B. Q2:= Q1 # X# Q3 C. Q2:= Q1 & amp; X & amp; Q3 D. Q2:= Q1 & X L Q3
133	Caveman number system is Base number system	A. 2 B. 5 C. 10 D. 16
134	The output of an XOR gate is zero (0) when I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one.	A. I Only B. IV Only C. I and IV only D. II and III only
135	The decimal "17" in BCD will be represented as10001(right opt is not given)	A. 11101 B. 11101 C. 10111 D. 11110
136	The simplest and most commonly used Decoders are the Decoders	A. n to 2n-1 B. n to 2n C. (n-1) to 2n D. (n-1) to (2n-1)
137	The simplest and most commonly used Decoders are the Decoders	A. (n-1) to (2n-1) B. (n-1) to 2n C. n to 2n-1 D. n to 2n
138	The Encoder is used as a keypad encoder.	A. 2-to-8 encoder B. 4-to-16 encoder C. BCD-to-Decimal D. Decimal-to-BCD Priority
139	If the S and R inputs of the gated S-R latch are connected together using agate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)	A. AND B. OR C. NOT D. XOR
140	The low to high or high to low transition of the clock is considered to be a(n)	A. State B. Edge C. Trigger D. One-shot
141	RCO Stands for	A. Reconfiguration Counter Output B. Reconfiguration Clock Output C. Ripple Counter Output D. Ripple Clock Output
142	A transparent mode means	 A. The changes in the data at the inputs of the latch are seen at the output B. The changes in the data at the inputs of the latch are not seen at the output C. Propagation Delay is zero (Output is immediately changed when clock signal is applied) D. Input Hold time is zero (no need to maintain input after clock transition)
143	In outputs depend only on the current state	A. Mealy machine B. Moore Machine C. State Reduction table D. State Assignment table
144	In asynchronous transmission when the transmission line is idle,	A. It is set to logic lowB. Remains in previous stateC. It is set to logic highD. State of transmission line is not used to start transmission
145	Smallest unit of binary data is a	A. Bit B. Nibble

C. Previous data is swapped out of

		D. Word
146	Excess-8 code assigns to "+7"	A. 0000 B. 1001 C. 1000
147	NOR gate is formed by connecting	D. 1111 A. OR Gate and then NOT Gate B. NOT Gate and then OR Gate C. AND Gate and then OR Gate D. OR Gate and then AND Gate